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# Question Paper Code : 42441

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2018

Third Semester

Electronics and Communication Engineering

EC 2203 – DIGITAL ELECTRONICS

(Regulations 2008)

(Common to PTEC 2203 – Digital Electronics for B.E. (Part-Time) Third Semester – ECE – Regulations 2009)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Express x + yz as the sum of minterms.
2. What is meant by wired logic ?
3. State the condition to check the equality of two n-bit binary numbers A and B.
4. How can a DEMUX be used as a decoder ?
5. With reference to a JK flip-flop, what is meant by racing ?
6. When is a counter said to suffer from lockout ?
7. How many data inputs, data outputs and address inputs are needed for a 1024 × 4 ROM ?
8. Distinguish between PAL versus PLA.
9. Define Essential Hazard and how it can be avoided ?
10. Distinguish between fundamental mode circuits versus pulse-mode circuits.

PART – B **(5×16=80 Marks)**

11. a) i) Draw a logic diagram using only two-input NOR gates to implement the following function : $F(A, B, C, D) = (A \oplus B)'. (C \oplus D)$. **(8)**

ii) Implement the following Boolean function F, together with the don't-care conditions d, using not more than two NOR gates :

$F(A, B, C, D) = \Sigma (2, 4, 6, 10, 12)$

$d(A, B, C, D) = \Sigma (0, 8, 9, 13)$

Assume that both the normal and complement inputs are available. **(8)**

(OR)

b) Explain the Tri-State TTL configuration with neat diagram. **(16)**

12. a) i) With a neat diagram, explain in detail about the working of a 4-bit look ahead carry adder. Also mention its advantage over conventional adder. **(10)**

ii) Specify the truth table of an octal-to-binary priority encoder and explain the operation. **(6)**

(OR)

b) i) Briefly explain the working of a 2-bit by 2-bit binary multiplier with neat sketches. **(8)**

ii) Construct a 4 to 16 line decoder with five 2 to 4 line decoders with enable. **(8)**

13. a) Draw the logic diagram of a 4-bit universal shift register and explain the operation of the circuit. **(16)**

(OR)

b) Design a synchronous BCD counter using JK flip-flops. Comment on whether the counter is self starting. **(16)**

14. a) i) Design a combinational circuit using a PROM. The circuit accepts a 3-bit binary number and generates its equivalent XS-3 code. **(8)**

ii) Construct the logic circuit of a RAM memory cell using SR flip-flop and explain the working. **(8)**

(OR)

b) Write the program table to implement a BCD to Excess-3 code conversion using a PLA. **(16)**

15. a) i) A sequential circuit with two D flip-flops A and B. Two inputs x and y and one output z is specified by the following next-state and output equations.

$A(t + 1) = x'y + x B$

$B(t + 1) = x'A + xB$

$z = A$

Draw the logic diagram, state table and state diagram of the circuit. **(10)**

ii) Briefly explain the race free state assignment by taking a three row flow table example. **(6)**

(OR)

b) Design an asynchronous negative-edge-triggered T flip-flop. The circuit has two inputs, T (toggle) and C (clock) and one output, Q. The output state is complemented if T = 1 and the clock C changes from 1 to 0 (negative-edge triggering). Otherwise, under any other input condition, the output Q remains unchanged. Construct the designed circuit using SR latch. **(16)**